Stud Bump Process for Flip Chip Package

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Abstract

This work proposes one way to interconnect the chip inverted to the thin film substrate (flip chip) through mechanical attachment of the gold (Au) stud bumps electrical connection, it also reduces the footprint and parasitics from the circuit. This flip chip mechanism allows fast, simple deployment at any service scale in the Electronic Packaging Research Group at Renato Archer Center for Information Technology.

Keywords: Flip Chip, Package, Gold Stud Bumps.

1. Introduction

Heterogeneous Integration is and will be the key technology direction going forward. Therefore, new packaging designers are looking toward Au bumps as a chip interconnects solution in front as power requirements and operating frequencies increase. Stud bumps offers finer bump spacing than most solder bump technology without the added expense of a solder re-distribution layer. It is possible to get flip chip with reduced chip area on substrate, compact modules, reduced cost, interconnect hidden below silicon; the lower inductance, highest frequency, best noise control due to shorter interconnect path and parallel bonding of all signals [1-7].

2. Experimental Procedure

In Au stud bump process an Au-wire sticks out of a capillary from the tool and a high-voltage-spark melts the wire (“flame-off”). Surface tension forms a free-air-ball on the very tip of the exposed wire, which is pulled back against the capillary and pressed onto Au-bondpad to form the bump. Ultrassonic and heat are used to form Au-Au interconnection. The wire is then sheared-off and ripped-off near the bump. For the bump formation tests performed on this paper the following parameters have been studied: Ultrasonic power (mW); Time (ms); Force (mN); Tail Height – Height where the wire tear off (µm); Tear Motion – Traverse motion of the toold to tear off the wire (µm); Tear Counter – Number of sideways movements to break the wire.

For this work, 2" <100> Si wafers were coated with 200 nm of Au by sputtering and cut into 5x5 mm squares to simulate an actual chip. Au stud bumps were placed onto these chips using modified wire bonding processes/recipes using the EMEA F&S Bondtec – Delvotec 5610. After recipe calibration, three rounds of one hundred stud bumps each were performed to extract the dimensions. Each sample was characterized using the SEM-FIB of CCSNano/Unicamp for evaluating the reproducibility of the process. Then we will decrease the thickness of the used wire from 25 µm to 17 µm.

3. Results and Discussion

The objective of the work is to evaluate and reduce variations in the stud bumps process. Therefore, in Table 1 it is possible to observe details of the parameters configuration for ball bumps formed. These parameters determined the required specifications of the stud bumps for Daisy Chain structures.

Parameters	
US (mW)	80
Time (ms)	90
Force (mN)	15
Tail Height (µm)	30
Tear Motion (µm)	60
Tear Counter	3

Table 1: The best parameters configuration obtained.

The Table 2 show details of the ball bumps formed by parameters application. This recipe provides an excellent correlation between the maximum and minimum values with the average, presented by the standard deviation values. In the Figure 1 are demonstrated the positions of the diameter, total height, and base height, essentials for evaluating the reproducibility of the process. The measures will determine the specifications of the device pads.

	Number of Samples	Avarage (µm)	Standard Deviation (µm)	Maximum (µm)	Minimum (µm)
Diameter	100	96.40	3.41	108.25	91.50
Total Height	100	74.55	3.27	81.87	67.87
Base Height	100	22.29	1.87	25.70	17.45

Table 2: Diameters and heights measures of samples set obtained through the be parameters configuration.

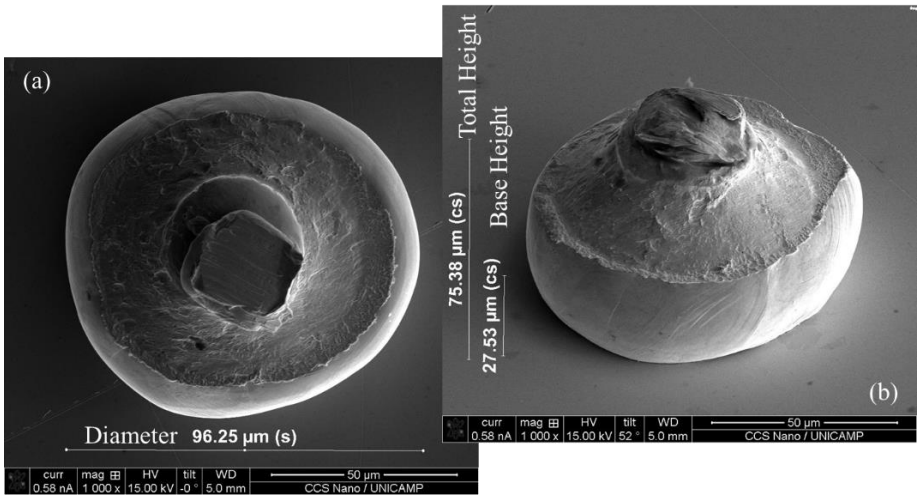

Figure 1: The positions of the (a) diameter, (b) total height, and (b) base height for extraction of the dimensions.

The Figures 2(a), 2(b) and 2(c) below shows the results of the developed process. It is possible to observe the details of the ball bumps formed by best configuration of the parameters. In this case, the stud bumps are positioned correctly in the Daisy Chain structures for thermocompression tests.

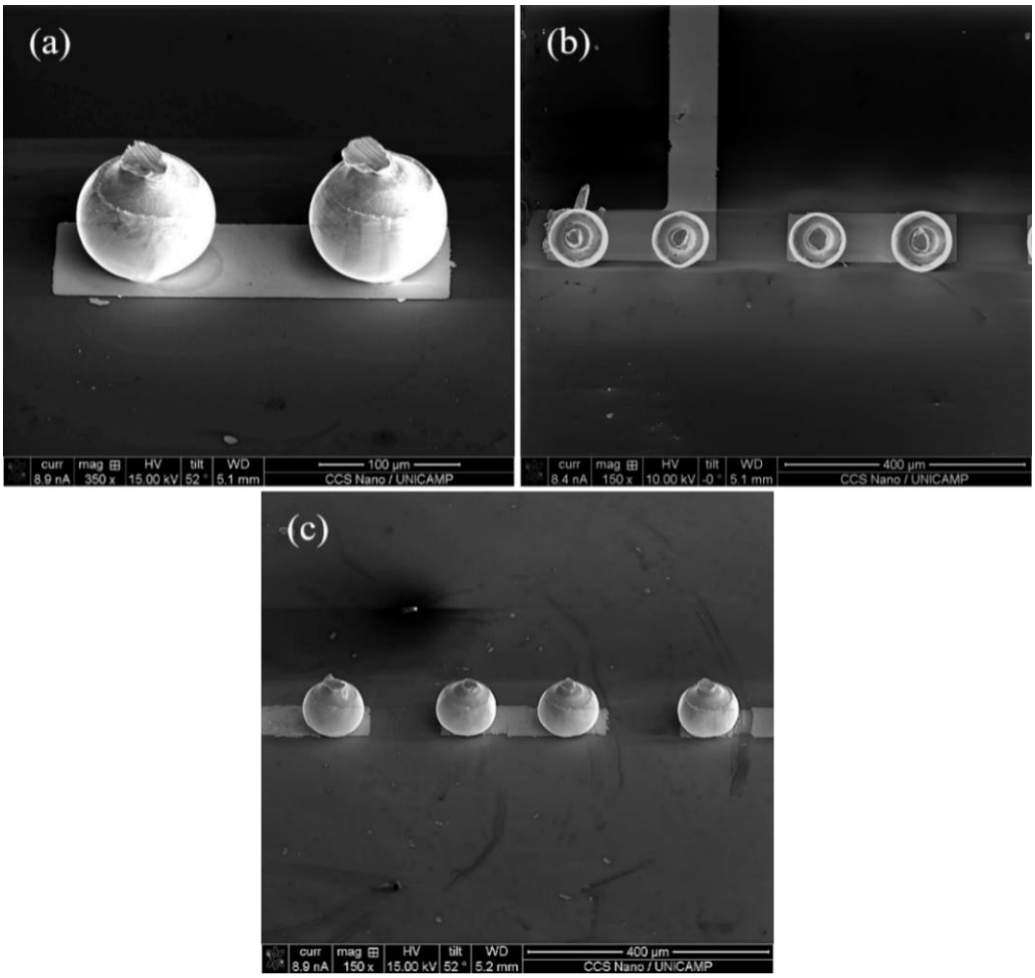

Figure 2: Results for parameters in use to development Au stud bumps on the EMEA F&S Bondtec – Delvotec 5610.

4. Conclusions

In this paper we showed the Au stud bump process to development a usual recipe without the coining step, the principal difference in relation to traditional processes. The Flip chip technology is now available at DIMES/CTI and the functional recipe will be studied for process optimization. Once completed, this service will be available to the scientific and industrial community.

5. Acknowledgments

CNPq and FINEP for the financial support; CCSNanano for the characterization support; Ednan Joani, Melissa Vidal and Alexander Flacker for helping on sample preparation.

6. References

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