Gold Stud Bumps for Flip Chip Technology

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Abstract

Gold stud bumps requires no Under Bump Metallization (UBM) preprocessing or special wafer preparation, unlike the requirements for solder bumping. It also offers finer bump spacing than most solder bump technology without the added expense of a solder re-distribution layer. Au stud bumps can be produced in a wide variety of diameters and shapes depending on the flip chip application. It is possible to get a flip chip with reduced chip area on the substrate; compact modules; robust modules; interconnect hidden below silicon, underfill; lower inductance due to shorter interconnect path and parallel bonding of all signals.

Keywords: Package, Flip Chip, Gold Stud Bumps.

1. Introdution

Flip Chip Technology is an advanced form of surface mount technology, in which bare semiconductor chips are turned upside down, and hence called flip chip (i.e active face down), and bonded directly to a Printed circuit Board or Chip Carrier Substrate Flip Chip technology is expected to reach $25 billion market value and wafer demand of 32 million in 2020. Flip Chip solutions have been largely adopted towards the mobile-wireless, consumer and computing applications, including continuous growth in the LED and CMOS Image Sensor (CIS) segments. That growth will be led by Moore's law pushing beyond the 28nm node and 'More than Moore' evolution in next-generation DDR and 3DICs (YOLE, 2019; BEICA, 2013)

To eliminate the expense, unreliability and low productivity of wire bonding. Eliminating packages and bond wires reduces the required board area by up to 95%, and requires far less height. Weight can be less than 5% of packaged device weight. Flip chip is the simplest minimal package, smaller than Chip Scale Packages (CSP's) because it is chip size. Self-aligning chip's bump pattern to corresponding substrate pad. Shortest possible leads, lowest inductance, highest frequency, best noise control, highest density and reduced cost (WANG, 2007).

Gold stud bumps can be used on individual die or wafer and typically have much lower set-up costs than a solder bump approach. The ability to bump individual die makes Au stud bumping an extremely valuable tool in the prototyping phase, as well as a viable option for volume manufacturing (FINETECH, 2019). Typically used for applications that requires a finer pitch than solder bump technology. These finer pitches enable greater functionality to be integrated onto a chip while maintaining a small form factor. A mainstream application of gold stud bumps is for surface acoustic wave (SAW) filters used in mobile phones and other radio frequency (RF) applications. For many sensitive devices such as lasers, MEMS and sensors the use of flux or adhesives is not allowed and a thermosonic or thermocompression Au-Au attach method offers a flux free process to improve the device reliability (FINETECH, 2019; OPTOCAP, 2019).

The Au stud bumps proposed in this project is one of the ways to interconnect the chip inverted to the substrate ("flip"), while providing mechanical attachment and electrical connection between the two elements, chip and substrate, which facilitates its implementation and is more appropriate to the type of service normally requested by the Electronic Packaging Research Group (Núcleo de Empacotamento Eletrônico – NEE) at Renato Archer Information Technology Center.

2. Experimental Procedure

Gold stud bumping is a technique for creating conductive gold bumps on a die bond pad which ultimately enable the die to be electrically interconnected to a package or substrate through thermo-compression or thermo-sonic flip chip attach process (VALLEJO, 2019). Au stud bumping uses a modified wire bond process, whereby the Au ball is formed on the die bond pad, as in wire bonding, but instead of spooling the wire to a package or substrate, the wire is cut just above the ball to leave a stud bump on the die bond pad.

In this work, 2" <100> Si wafers were coated with 200nm of Au by sputtering and cut into 5x5mm squares to chip simulate. Au stud bumps were made on the chips using modified wire bonding processes/recipes using the EMEA F&S Bondtec – Delvotec 5610.

3. Results and Discussion

Initial welding tests were done using basic parameters found in the literature (FINETECH, 2019; TSAO *at al*, 2016; REN *at al*, 2016). Next steps include tests to define the process for Au stud bumps Flip Chip in a reproductive way for the present test vehicle and evaluate the load (force) required as a function of the bump array dimensions and geometry (without tail in the ball). In this case, the Au-wire sticks out of capillary; high-voltage-spark melts wire (“flame-off”); surface tension forms free-air-ball; vacuum pulls the ball to capillary; capillary presses ball onto Au-bond pad and forms bump; ultrasonic to form Au-Au interconnection; shear-off wire near the bump and pull up capillary and rip off. For the recipes the following parameters have been changed: Ultrasonic (mW); Time (ms); Force (mN); Tail Height – Height where the wire tear off (µm); Tear Motion – Traverse to tear off the wire; Tear Counter – Number of sideways movements to break the wire. In Table 1 it is possible to observe details of the ball bumps formed by parameters variation. These measures will determine the required specifications of the device pads.

	Number of Samples	Average (µm)	Standard Deviation (µm)	Maximum (µm)	Minimum (µm)
Diameter	100	96.40	3.41	108.25	91.50
Total Height	100	74.55	3.27	81.87	67.87
Base Height	100	22.29	1.87	25.70	17.45

Table 1: Diameters and heights measures of samples set obtained through the best parameters configuration.

The inspections will be conducted on X-ray analysis to look for non-bonded areas and, cross-section to evaluate the high loss of the bumps due to the Flip Chip process. The results will allow fine tuning of the Flip Chip process. Subsequently, the assemblies will be scaled to more complex geometries such as daisy chains and interconnect arrays for electrical characterization. The final test vehicle will be to assemble actual and functional devices on a dedicated substrate, comparing electrical parameters and other figures-of-merit before and after the Flip Chip is done.

The Figures 1(a),1(b) and 1(c) below shows the results for parameters that are being used as the basis for the processes (recipes) development. It is possible to observe the conformation details of the ball bumps.

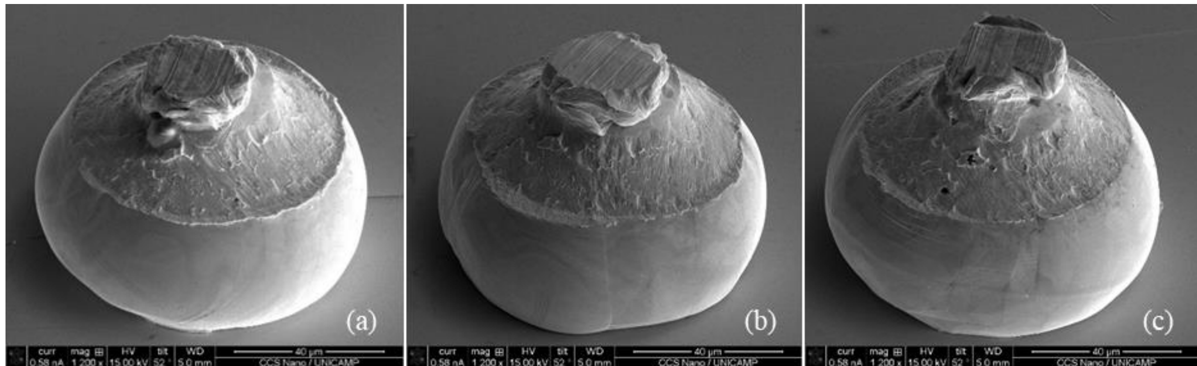

Fig. 1. Results for parameters in use to development Au stud bumps on the EMEA F&S Bondtec – Delvotec 5610.

4. Conclusions

In this paper, we showed the Au stud bump process to develop a usual recipe. The Flip Chip technology is now available at NEE/CTI and the functional recipe will be development for process optimization. Once completed, this service will be available to the scientific and industrial community.

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